Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1 - 16 (canceled)

Claim 17 (canceled)

18. (currently amended) A matrix panel display apparatus according to claim [[17]] 23 or 24, wherein said display medium is a liquid crystal.

19. (currently amended) A matrix panel display apparatus according to claim [[17]] 23 or [[18]] 24, wherein in each of said first image signal group and said second image signal group, the polarity of said image signals are reversed in successive frames.

20. (currently amended) A matrix panel display apparatus according to claim [[17]] 23 or [[18]] 24, wherein the number of said first group of picture elements nearly equals the number of said second group of picture elements.

21. (currently amended) A matrix panel display apparatus according to claim [[17]] 23 or [[18]], wherein each picture element group consisting of the picture elements of every n column elements ($n \geq 1$) is alternately assigned to said first group of picture elements and said second group of picture elements, respectively.

22. (currently amended) A matrix panel display apparatus according to claim ~~17 or 18~~ 24, wherein a control terminal of each transistor is connected to a scanning line, a

main terminal thereof to a signal line, and the other main terminal thereof to one of the terminals of said picture element electrode and said storage capacitance; and

wherein two groups of said bias signals, having a polarity reverse to each of said two image signal groups, are applied to said storage capacitances in each of said picture element groups, respectively.

23. (currently amended) A matrix panel display apparatus ~~according to claim 22,~~ comprising:

plural signal lines and plural scanning lines intersecting each other and, near each intersection point, a picture element including a picture element electrode, a counter electrode, a display medium disposed between said picture element electrode and said counter electrode, and a transistor for applying image signals from said signal line to said picture element electrode, said transistor being controlled in response to scanning signals received on a scanning line;

a plurality of storage capacitances, each connected to a respective one of said picture elements;

picture signal generating means in a signal circuit for dividing plural picture elements selected at the same time into two groups and for applying a first picture signal group to a first group of picture elements and a second picture signal group, having a polarity reverse to the first picture signal group, to a second group of picture elements;

bias signal generating means for applying a first bias signal group, having a polarity reverse to said first picture signal group, to said first group of picture elements through storage capacitances in said first group of picture elements and for applying a second bias signal group, having the polarity reverse to said second picture signal group, to said second group of picture elements through storage capacitances in said second group of picture elements, during a selection period of said first and second groups of picture elements;

wherein a control terminal of each transistor is connected to a scanning line, a main terminal thereof to a signal line, and the other main terminal thereof to one of the terminals of said picture element electrode and said storage capacitance; and

wherein two groups of said bias signals, having a polarity reverse to each of said two image signal groups, are applied to said storage capacitances in each of said picture element groups, respectively; and

wherein said bias signal generating circuit includes a scanning signal generating circuit for applying a scanning voltage to said picture element through said scanning lines.

24. (currently amended) A matrix panel display apparatus ~~according to claim 17 or 18,~~ comprising:

plural signal lines and plural scanning lines intersecting each other and, near each intersection point, a picture element including a picture element electrode, a counter electrode, a display medium disposed between said picture element electrode and said counter electrode, and a transistor for applying image signals from said signal line to said picture element electrode, said transistor being controlled in response to scanning signals received on a scanning line;

a plurality of storage capacitances, each connected to a respective one of said picture elements;

picture signal generating means in a signal circuit for dividing plural picture elements selected at the same time into two groups and for applying a first picture signal group to a first group of picture elements and a second picture signal group, having a polarity reverse to the first picture signal group, to a second group of picture elements;

bias signal generating means for applying a first bias signal group, having a polarity reverse to said first picture signal group, to said first group of picture elements through storage capacitances in said first group of picture elements and for applying a second bias signal group, having the polarity reverse to said

second picture signal group, to said second group of picture elements through storage capacitances in said second group of picture elements, during a selection period of said first and second groups of picture elements;

wherein a terminal of a storage capacitance belonging to said first group of picture elements is connected to a scanning line which is located one line before a line being scanned presently;

wherein a terminal of a storage capacitance belonging to said second group of picture elements is connected to a scanning line which is located one line behind a line being scanned presently;

wherein said bias signal generating means operates to apply a first bias signal to a scanning line which is located one line before a line being scanned presently and to apply a second bias signal of the polarity reverse to said first bias signal to a scanning line which is located one line behind a line being scanned presently, while one scanning line is selected; and

wherein said apparatus further comprises an image signal generating circuit which applies image signals having a polarity reverse to said first bias signal to said first group of picture elements and image signals having the polarity reverse to said second bias signal to said second group of picture elements.

25. (previously presented) A matrix panel display apparatus according to claim 24, wherein each picture element group consisting of picture elements of every n column elements ($n \geq 1$) is alternately assigned to said first group of picture elements and said second group of picture elements, respectively.

26. (previously presented) A matrix panel display apparatus according to claim 24, wherein said scanning signal generating circuit generates bias voltages such that, when a scanning pulse is applied to said scanning line, each polarity of said first bias signal and said second bias signal applied to said scanning line is constant independently of said scanned line in one frame period.

27. (previously presented) A matrix panel display apparatus according to claim 24, further comprising a scanning signal generating circuit which generates bias voltages such that, when a scanning pulse is applied to said scanning line, the polarity of said first bias signal group and said second bias signal group applied to said scanning line is alternately reversed as said scanning pulse transfers in turn on said scanning lines;

wherein said image signal generating circuit generates image signals so that the polarity of said first image signal and said second image signal is alternately reversed in every scanning period as said scanning pulse transfers in turn on said scanning lines.

28. (previously presented) A matrix panel display apparatus according to claim 24, wherein said image signal generating circuit includes:

a first image signal generating part for applying image signals to a first group of picture elements; and

a second image signal generating part for applying image signals to a second group of picture elements.

29. (previously presented) A matrix panel display apparatus according to claim 24, wherein said image signal generating circuit includes:

a first latch for storing image signals in turn;

a second latch for storing image signals which are synchronized with a horizontal synchronizing signal;

a third latch capable of either latching said image signals or passing said image signals; and

a sample hold circuit for generating said image signals.

30. (previously presented) A matrix panel display apparatus according to claim 24, wherein said scanning circuit executes interlaced scanning.

31. (original) A matrix panel display apparatus according to claim 24, wherein each electrode of said first group of picture elements partially overlaps with each electrode of said second group of picture elements in the column direction.

32. (original) A matrix panel display apparatus according to claim 24, wherein said first group of picture elements consists of odd column picture elements and said second group of picture elements consists of even column picture elements.

33. (previously presented) A computer system comprising a matrix panel display apparatus according to claim 24.

Claim 34 (canceled)